Beceipt date: 10/02/2008

10550326 - FALL: 2439

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 08/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE	Application Number		10550326	
	Filing Date		2005-09-23	
	First Named Inventor Roger		r D. Chamberlain	
(Not for submission under 37 CFR 1.99)	Art Unit		2131	
(Not for Submission ander or of it mos)	Examiner Name			
	Attorney Docket Number		53047-57365	

				U.S.I	PATENTS	Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	3601808		1971-08-24	Vlack	
	2	3611314	A	1971-10-05	Pritchard, Jr. et al.	
	3	3729712	A	1973-04-24	Glassman	
	4	3824375	A	1974-07-16	Gross et al.	
	5	3848235	A	1974-11-12	Lewis et al.	
	6	3906455	A	1975-09-16	Houston et al.	
	7	4081607	A	1978-03-28	Vitols et al.	
	8	4298898	A	1981-11-03	Cardot	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.T./ (05/26/2010)

Receipt date: 10/02/2008		Application Number			10550326	1055	0326 -	GAU: 2439		
				Filing Date			2005-09-23			
		TION DISCLOSU		First Named Inventor Roger		r D. Chamberlain				
		NT BY APPLICA ission under 37 CFR 1.		Art Unit			2131			
(NOT IOF :	aupiili	ission under 37 OFK 1.	.33)	Examiner Na	me		•			
				Attorney Doc	ket Numb	er	53047-57365			
	9	4314356	А	1982-02-02	Scarbroug	h				
	10	4385393	A	1983-05-24	Chaure et	al.				
	11	4464718	A	1984-08-07	Dixon et a	l.				
	12	4550436	A	1985-10-29	Freeman e	et al.				
	13	4823306	А	1989-04-18	Barbic et a	ıl.				
If you wis	h to ac	dd additional U.S. Paten	t citatio	n information pl	ease click	the A	dd button.		Add	
			U.S.P.	ATENT APPLI	CATION P	UBLIC	CATIONS		Remove	
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of of cited D		tee or Applicant ent		it Passag	Lines where les or Relevant
	1	20020082967	A1	2002-06-27	Kaminsky	et al.				
	2	20030055658	A1	2003-03-20	RuDusky					
	3	20030055770	A1	2003-03-20	RuDusky					
	4	20030055771	A1	2003-03-20	RuDusky					
		ALL REFERENCES	CONS	IDERED EXCI	EPT WHE	RE LI	NED THROUGH	4. /R.T./	(05/26/2	2010}

Receipt date: 10/02/2008 10550326 - GAU: 2439 Application Number 10550326 Filing Date 2005-09-23

INFORMATION BIGGLOOUSE	1 lillig Date		2000-00-20	
INFORMATION DISCLOSURE	First Named Inventor	Roge	r D. Chamberlain	
(Not for submission under 37 CFR 1.99)	Art Unit	•	2131	
(Not for Submission under 57 Of K 1.33)	Examiner Name			
	Attorney Docket Number		53047-57365	

	<u>, </u>				
5	20030093347	A1	2003-05-15	Gray	
6	20030126065	A1	2003-07-03	Eng et al.	
7	20040034587	A1	2004-02-19	Amberson et al.	
8	20040177340		2004-09-09	Hsu et al.	
9	20040186804	A1	2004-09-23	Chakraborty et al.	
10	20040186814	A1	2004-09-23	Chalermkraivuth et al.	
11	20040199448	A1	2004-10-07	Chalermkraivuth et al.	
12	20050033672	A1	2005-02-10	Lasry et al.	
13	20050091142	A1	2005-04-28	Renton et al.	
14	20050131790	A1	2005-06-16	Benzschawel et al.	
15	20050187844	A1	2005-08-25	Chalermkraivuth et al.	
	ALL REFERENC	ES CO	NSIDERED EX	CEPT WHERE LINED THROU	IGH. /R.T./ (05/26/2010)

Receipt date: 10/02/2008 10550326 - GAU: 2439 Application Number 10550326 Filing Date 2005-09-23 INFORMATION DISCLOSURE First Named Inventor Roger D. Chamberlain 2131 Art Unit (Not for submission under 37 CFR 1.99) **Examiner Name**

53047-57365

Attorney Docket Number

IN OKNATION DISCLOSUKE	
STATEMENT BY APPLICANT	

1	16	20050187845	A1	2005-08-25	Eklund et al.	
1	17	20050187846	A1	2005-08-25	Subbu et al.	
1	18	20050187847	A1	2005-08-25	Bonissone et al.	
1	19	20050187848	A1	2005-08-25	Bonissone et al.	
2	20	20050187849	A1	2005-08-25	Bollapragada et al.	
2	21	20050197938	A1	2005-09-08	Davie et al.	
2	22	20050197939	A1	2005-09-08	Davie et al.	
2	23	20050197948	A1	2005-09-08	Davie et al.	
2	24	20050216384	A1	2005-09-29	Partlow et al.	
2	25	20050267836	A1	2005-12-01	Crosthwaite et al.	
2	26	20050283423	A1	2005-12-22	Moser et al.	

Receipt date: 10/02/2008 10550326 - GAU: 2439 **Application Number** 10550326 Filing Date 2005-09-23 **INFORMATION DISCLOSURE** First Named Inventor Roger D. Chamberlain 2131 Art Unit (Not for submission under 37 CFR 1.99)

STATEMENT BY APPLICA	١T
/N /	

Not for Submission under 67 of it 1.33,	Examiner Name		
	Attorney Docket Number	er	53047-57365

			ı			
2	27	20060020536	A1	2006-01-26	Renton et al.	
2	28	20060031154	A1	2006-02-09	Noviello et al.	
2	29	20060031156	A1	2006-02-09	Noviello et al.	
3	30	20060059064	A1	2006-03-16	Glinberg et al.	
3	31	20060059065	A1	2006-03-16	Glinberg et al.	
3	32	20060059066	A1	2006-03-16	Glinberg et al.	
3	33	20060059067	A1	2006-03-16	Glinberg et al.	
3	34	20060059068	A1	2006-03-16	Glinberg et al.	
3	35	20060059069	A1	2006-03-16	Glinberg et al.	
3	36	20060059083	A1	2006-03-16	Friesen et al.	
3	37	20060143099	A1	2006-06-29	Partlow et al.	

Receipt date: 10/02/2008	Application Number		10550326	10550326	- GAU: 2439
Receipt date: 10/02/2008 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Filing Date		2005-09-23		
	First Named Inventor Roger		r D. Chamberlain		
	Art Unit		2131		
(Not lot Submission under or of N 1.00)	Examiner Name				
	Attorney Docket Numb	er	53047-57365		

If you wisl	n to ac	dd additional U.S. Pub	lished Application	n citation	n information	please click the Add butto	on. Add	
			FOREI	GN PAT	ENT DOCUM	IENTS	Remove	
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T5
	1	0851358	EP	A	1998-07-01	Sun Microsystems Inc		
	2	0880088	EP		1998-11-25	Mitsubishi Corporation		
	3	0887723	EP		1998-12-30	International Business Machines Corporation		
	4	0911738	EP	A	1999-04-28	Calluna Technology Ltd		
	5	0122425	wo	A	2001-03-29	Seagate Technology LLC		
	6	05017708	wo		2005-02-24	Washington University		
If you wisl	n to ac	dd additional Foreign F	Patent Document	citation	information p	lease click the Add buttor	Add	
			NON-PATE	NT LITE	RATURE DO	CUMENTS	Remove	
Examiner Initials*	Cite No		rnal, serial, symp	osium,	catalog, etc),	the article (when approportion that the date, pages(s), volume-is		T 5
	1		chnologies Press F			s for Programmable, Multi-F om http://www.lucent.com/pr		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.T./ (05/26/2010)

Receipt date: 10/02/2008	Application Number		10550326	10550326 - GAU: 2439
INFORMATION BIOCH COURT	Filing Date		2005-09-23	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	First Named Inventor	Roger	D. Chamberlain	
	Art Unit		2131	
(Notion Submission under or of it 1.00)	Examiner Name			
	Attorney Docket Numb	er	53047-57365	

2	"Overview, Field Programmable Port Extender", January 2002 Gigabit Workshop Tutorial, Washington University, St. Louis, MO, January 3-4, 2002	
3	"Payload PlusTM Agere System Interface", Agere Systems Product Brief, June 2001, downloaded from Internet, January 2002	
4	"The Field-Programmable Port Extender (FPX)", downloaded from http://www.arl.wustl.edu/arl/ in March 2002	
5	ANONYMOUS; "Method for Allocating Computer Disk Space to a File of Known Size", IBM Technical Disclosure Bulletin, Vol. 27, No. 10B, March 1, 1985, New York	
6	ARNOLD et al.; "The Splash 2 Processor and Applications"; Proceedings 1993 IEEE International Conference on Computer Design: VLSI In Computers and Processors (ICCD '93); October 3, 1993; pp 482-485; IEEE Computer Society; Cambridge, MA USA	
7	BAER, JEAN-LOUP; "Computer Systems Architecture"; 1980; pp. 262-265; Computer Science Press; Potomac, Maryland	
8	BAEZA-YATES and NAVARRO, "New and Faster Filters for Multiple Approximate String Matching", Random Structures and Algorithms (RSA) Vol. 20, No. 1, January 2002, pp. 23-49.	
9	BERK, Elliott, "JLex: A lexical analyzer generator for JavaTM", downloaded from http://www.cs.princeton.edu/~appel/modern/java/Jlex/ in January 2002 pp. 1-18	
10	BRAUN et al., "Layered Protocol Wrappers for Internet Packet Processing in Reconfigurable Hardware", Proceedings of Hot Interconnects 9 (Hotl-9) Stanford, CA, August 22-24, 2001, pp. 93-98	
11	CHOI et al., "Design of a Flexible Open Platform for High Performance Active Networks", Allerton Conference, Champaign, II, 1999	
12	CLOUTIER et al.; "VIP: An FPGA-Based Processor for Image Processing and Neural Networks"; Proceedings of Fifth International Conference on Microelectronics for Neural Networks; February 12, 1996; pp. 330-336; Los Alamitos, California	

Receipt date: 10/02/2008 10550326 - GAU: 2439 Application Number 10550326 Filing Date 2005-09-23 INFORMATION DISCLOSURE First Named Inventor Roger D. Chamberlain 2131 Art Unit (Not for submission under 37 CFR 1.99) **Examiner Name**

Attorney Docket Number

53047-57365

1141		117	110	.14 -	,,,,,,			17
STA	ATE	ΜE	NT	BY	AF	PL	ICA	NT

13	COMPTON et al.; "Configurable Computing: A Survey of Systems and Software"; Technical Report, Northwestern University, Dept. of ECE, 1999	
14	CONG et al., An Optional Technology Mapping Algorithm for Delay Optimization in Lookup-Table Based FPGA Designs, IEEE, 1992, 48-53.	
15	EBELING et al. "RaPiD - Reconfigurable Pipelined Datapath", University of Washington, Dept. of Computer Science and Engineering, September 23, 1996; Seattle, WA	
16	FRANKLIN et al., "Assisting Network Intrusion Detection with Reconfigurable Hardware", Symposium on Field-Programmable Custom Computing Machines (FCCM 2002), April 2002, Napa, California	
17	FU et al., "The FPX KCPSM Module: An Embedded, Reconfigurable Active Processing Module for the Field Programmable Port Extender (FPX)", Washington University, Department of Computer Science, Technical Report WUCS-01-14, July, 2001	
18	GAVRILA et al., "Multi-feature Hierarchical Template Matching Using Distance Transforms", IEEE, Aug. 16-20, 1998, Vol. 1, pp. 439-444.	
19	GUNTHER et al., "Assessing Document Relevance with Run-Time Reconfigurable Machines", FPGAs for Custom Computing Machines, 1996, Proceedings, IEEE Symposium on Napa Valley, CA, April 17, 1996	
20	HAUCK et al., "Software Technologies for Reconfigurable Systems", Northwestern University, Dept. of ECE, Technical Report, 1996	
21	HAYES, "Computer Architecture and Organization", Second Edition, 1988, pp. 448-459, McGraw-Hill, Inc.	
22	HEZEL et al., "FPGA-Based Template Matching Using Distance Transforms", Proceedings of the 10th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, April 22, 2002, pp. 89-97; IEEE Computer Society, USA	
23	HOLLAAR, "Hardware Systems for Text Information Retrieval", Proceedings of the Sixth Annual International ACM Sigir Conference on Research and Development in Information Retrieval; June 6-8, 1983, pp. 3-9; Baltimore, Maryland, USA	

Receipt date: 10/02/2008	Application Number		10550326	10550326 -	GAU: 2439
	Filing Date		2005-09-23		
STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	First Named Inventor	Rogei	r D. Chamberlain		
	Art Unit		2131		
(Not lot Submission under or or it 1.00)	Examiner Name				
	Attorney Docket Numb	er	53047-57365		

24	International Search Report for PCT/US2001/011255; July 10, 2003	
25	International Search Report for PCT/US2003/015638; May 6, 2004	
26	International Search Report for PCT/US2004/016398; April 12, 2005	
27	KEUTZER et al., "A Survey of Programmable Platforms - Network Proc", University of California-Berkeley	
28	KULIG et al., "System and Method for Controlling Transmission of Data Packets Over an Information Network", pending U.S. Patent Application	
29	LOCKWOOD et al., "Field Programmable Port Extender (FPX) for Distributed Routing and Queuing", ACM International Symposium on Field Programmable Gate Arrays (FPGA 2000), Monterey, CA, February 2000, pp. 137-144	
30	LOCKWOOD et al., "Hello, World: A Simple Application for the Field Programmable Port Extender (FPX)", Washington University, Department of Computer Science, Technical Report WUCS-00-12, July 11, 2000	
31	LOCKWOOD et al., "Parallel FPGA Programming over Backplane Chassis", Washington University, Department of Computer Science, Technical Report WUCS-00-11, June 12, 2000	
32	LOCKWOOD et al., "Reprogrammable Network Packet Processing on the Field Programmable Port Extender (FPX)", ACM International Symposium on Field Programmable Gate Arrays (FPGA 2001), Monterey, CA, February 2001, pp. 87-93	
33	LOCKWOOD, J., "An Open Platform for Development of Network Processing Modules in Reprogrammable Hardware", IEC DesignCon 2001, Santa Clara, CA, January 2001, Paper WB-19	
34	LOCKWOOD, J., "Building Networks with Reprogrammable Hardware", Field Programmable Port Extender: January 2002 Gigabit Workshop Tutorial, Washington University, St. Louis, MO, January 3-4, 2002	
	ALL DEEDENACE CONCIDEDED EVACUT WHERE LINED TUDOUAL UDIT / (05/00/0040)	

Receipt date: 10/02/2008	Application Number		10550326	10550326	- GAU: 2439
INFORMATION BIGGI COURT	Filing Date		2005-09-23		
	First Named Inventor	Roge	r D. Chamberlain		
STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Art Unit		2131		
(not is submission and or or it not)	Examiner Name				

Attorney Docket Number

53047-57365

35	LOCKWOOD, J., "Evolvable Internet Hardware Platforms", NASA/DoD Workshop on Evolvable Hardware (EHW'01), Long Beach, CA, July 12-14, 2001, pp. 271-279	
36	LOCKWOOD, J., "Hardware Laboratory Configuration", Field Programmable Port Extender: January 2002 Gigabit Workshop Tutorial, Washington University, St. Louis, MO, January 3-4, 2002	
37	LOCKWOOD, J., "Introduction", Field Programmable Port Extender: January 2002 Gigabit Workshop Tutorial, Washington University, St. Louis, MO, January 3-4, 2002	
38	LOCKWOOD, J., "Platform and Methodology for Teaching Design of Hardware Modules in Internet Routers and Firewalls", IEEE Computer Society International Conference on Microelectronic Systems Education (MSE'2001), Las Vegas, NV, June 17-18, 2001, pp. 56-57	
39	LOCKWOOD, J., "Protocol Processing on the FPX", Field Programmable Port Extender: January 2002 Gigabit Workshop Tutorial, Washington University, St. Louis, MO, January 3-4, 2002	
40	LOCKWOOD, J., "Simulation and Synthesis", Field Programmable Port Extender: January 2002 Gigabit Workshop Tutorial, Washington University, St. Louis, MO, January 3-4, 2002	
41	LOCKWOOD, J., "Simulation of the Hello World Application for the Field-Programmable Port Extender (FPX)", Washington University, Applied Research Lab, Spring 2001 Gigabits Kits Workshop	
42	MOSANYA et al.; "A FPGA-Based Hardware Implementation of Generalized Profile Search Using Online Arithmetic"; ACM/Sigda International Symposium on Field Programmable Gate Arrays (FPGA '99); February 21-23, 1999; pp 101-111; Monterey, CA, USA	
43	MOSCOLA et al., "FPGrep and FPSed: Regular Expression Search and Substitution for Packet Streaming in Field Programmable Hardware", unpublished, pp. 1-19.	
44	NAVARRO, "A Guided Tour to Approximate String Matching", ACM Computing Surveys, Vol. 33, No. 1, March 2001, pp. 31-88.	
45	NUNEZ et al.; "The X-MatchLITE FPGA-Based Data Compressor", Euromicro Conference 1999, Proceedings, Italy, Sept. 8-10, 1999, Los Alamitos, CA	

Receipt date: 10/02/2008	Application Number		10550326	10550326	- GAU: 2439
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Filing Date		2005-09-23		
	First Named Inventor	Rogei	r D. Chamberlain		
	Art Unit		2131		
	Examiner Name				
	Attorney Docket Numb	er	53047-57365		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.T./ (05/26/2010)

	46 Partial International Search Report for PCT/US 03/15638 dated Feb. 3, 2004					
	PRAMANIK et al.; "A Hardware Pattern Matching Algorithm on a Dataflow"; Computer Journal; July 1, 1985; pp. 264-269; Vol. 28, No. 3; Oxford University Press, Surrey, Great Britain					
	RAMAKRISHNA et al., "A Performance Study of Hashing Functions for Hardware Applications", Journal of Computing and Information, Vol. 1, No. 1, May 1994, pp. 1621-1636.					
	49	RATHA et al.; "Convolution on Splash 2"; Proceedings of IEEE Symposium on FPGAS for Custom Computing Machines; April 19, 1995; pp. 204-213; Los Alamitos, California				
	SCHMIT; "Incremental Reconfiguration for Pipelined Applications"; Dept. of ECE, Carnegie Mellon University 1997, Pittsburgh, PA					
If you wis	h to ac	dd additional non-patent literature document citation information please click the Add button Add				
		EXAMINER SIGNATURE				
Examiner	Signa	ature /Roderick Tolentino/ (05/26/2010) Date Considered				
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						
Standard ST 4 Kind of doo	¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.					